Abstract of the Disclosure:

In a method for fabricating trench capacitors, in particular for memory cells having at least one selection transistor for integrated semiconductor memories, a trench for the trench capacitor is formed. The trench has a lower trench region, in which the capacitor is disposed, and an upper trench region, in which an electrically conductive connection from an electrode of the capacitor to a diffusion zone of the selection transistor is disposed. The method reduces the number of process steps for the fabrication of memory cells and enables fabrication of buried collars in the storage capacitors with an insulation quality as required for the fabrication of very large-scale integrated memory cells (<300 nm trench diameter).

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